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| 10/735,630 | 12/16/2003 | Isamu Ishimura | 61282-047 | 2674 |

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| EXAMINER | |
|---|---|
| VU, TRISHA U | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2112 | |

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/735,630 | ISHIMURA ET AL. | |
| | Examiner | Art Unit | |
| | Trisha Vu | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-11 are presented for examination.

### *Drawings*

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, ***the second contained CPU*** connected to ***the second bus*** wherein a bus adjusting circuit ***disposed between*** the first bus and the second bus in the LSI (e.g. claim 11) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. Claims 5-10 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend on any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Furuhashi et al. (6,180,864) (hereinafter Furuhashi '864').

As to claim 1, Furuhashi '864' teaches a CPU contained LSI (LSI 60) (Fig. 2 and col. 2 lines 65-67) comprising: a contained CPU (CPU 3, or any of DSPs 8-1 -> 8-4); a first bus (bus 12) connected to the contained CPU; a second bus (host bus 55) connected to an external CPU (CPU 57); and a bus adjusting circuit (bus arbiter 2 and associated circuitry such as host interface 1) disposed between the first bus and the second bus to exclusively control accesses of the external CPU and the contained CPU to a device (e.g. DRAM 5, DMAC 4, DSP 8-1, 8-2, ...) connected to the first bus and connect the second bus to the first bus only when the external CPU is permitted to access the device

connected to the first bus (e.g. when there is a request for data transfer from external host CPU 57 to DRAM 5) (Fig. 2 and col. 3 lines 4-25).

As to claim 11, Furuhashi '864' teaches a CPU contained LSI (LSI 60) comprising: a first contained CPU (one of DSPs 8-1 -> 8-4); a second contained CPU (CPU 3); a first bus (bus 12) connected to the first contained CPU; a second bus (bus 11) connected to the second contained CPU and a bus adjusting circuit (arbiter 2 and associated circuitry) disposed between the first bus and the second bus to exclusively control accesses of the second contained CPU (CPU 3) and the first contained CPU to a device (e.g. DRAM 5) connected to the first bus (12) and connect the second bus to the first bus only when the second contained CPU (CPU 3) is permitted to access the device connected to the first bus (by arbiter 2) (Fig. 2, col. 3 lines 4-59 and col. 5 lines 16-28).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (6,180,864) (hereinafter Furuhashi '864') in view of Falik et al. (6,532,507) (hereinafter Falik).

As to claim 2, the argument above for claim 1 applies. Furuhashi '864' teaches bus arbiter 2 to arbitrate the use rights to bus 12 e.g. when there is a request for data

transfer from external host CPU 57 to DRAM 5, bus arbiter 2 gives the bus access from CPU 57 to DRAM 5 (Fig. 2 and col. 3 lines 4-25). However Furuhashi '864' does not explicitly disclose how to handle a contention situation when there is a request for data transfer from the external host CPU 57 during which the contained CPU 3 has an access to the device (e.g. DRAM 5) connected to the bus 12. Falik teaches how to resolve access contention when there is a request for data transfer from one CPU (e.g. CPU 3 and associated circuitry) connected to a second bus (bus 4) to a device (e.g. RAM 9) connected to a first bus (bus 2) during which another CPU (CPU 1 and associated circuitry) has an access to the device (Figs. 1-2, col. 1 line 62 to col. 2 line 10, and col. 9 line 46 to col. 10 line 23). Specifically, Falik teaches in this situation, the bus arbiter (21) transmits a bus release request signal (Hold signal) to CPU 1 and transmits a wait signal (Wait signal) to CPU 3, and when the bus arbiter receives a bus release completion signal (Hold Acknowledge signal) from the CPU 1, the bus arbiter releases the wait signal to permit CPU 3 to access the device connected to the first bus (while waiting for CBC 8 to assert Hold Acknowledge signal to grant the request for control of bus 2, the arbiter stalls CPU 3 by sending Wait signal to BIC 5 (col. 1 line 62 to col. 2 line 10, and col. 9 line 46 to col. 10 line 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement transmitting a bus release request signal to the CPU having usage of the bus and transmitting a wait signal to the CPU requesting the bus, and releasing the wait signal to permit the requesting CPU to access the device connected to the bus after receiving a bus release completion signal as taught by Falik in the arbiter of Furuhashi '864' to resolve access contention when there is a request for

data transfer from one CPU during which another CPU has an access to the bus, and also to improve the throughput rate for inter-processor data transfer between a slow and a fast processor as shown in one of Falik's embodiment (col. 9 line 46 to col. 10 line 23).

As to claim 3, Furuhashi '864' further teaches when a stop of a operation of the contained CPU is set, the bus adjusting circuit permits the external CPU to access the device connected to the first bus without transmitting the bus release request signal to the contained CPU (this is inherent since if the contained CPU has stopped the operation, the contained CPU does not have data transfer operation on the bus, and thus there is no need to send out the bus release request to the contained CPU).

As to claim 4, Furuhashi '864' further teaches a common memory (e.g. DRAM 5) connected to the first bus is provided (Fig. 2).

As to claim 5, the argument above for claim 4 applies. Furuhashi '864' further teaches a memory device (e.g. DRAM 5, instruction cache 6, or program RAM 21-1 in DSP 8-1) connected to the first bus is provided for storing a program for operating the CPU contained LSI (Fig. 2 and col. 3 lines 26-65).

6. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (6,180,864) (hereinafter Furuhashi '864') in view of Falik et al. (6,532,507) (hereinafter Falik), and further in view of Moyer (6,845,419).

As to claim 6, the argument above for claim 5 applies. However, Furuhashi '864' and Falik do not disclose the bus adjusting circuit is provided with an interrupt control circuit for informing of an interruption between the contained CPU and the external CPU.

Falik teaches interrupt control circuit for informing of an interruption from a device or software to the main CPU (col. 1 lines 20-35 and col. 2 lines 54-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the interrupt control circuit as taught by Moyer in the system of Furuhashi '864' and Falik to provide the system with the ability to handle interrupts between LSI 60 and CPU 57 since interrupts are commonly used in computer systems to provide mechanism to force software to alter its current execution and perform talks that service the interrupt (col. 1 lines 20-22), and further to allow hardware (e.g. from a source in LSI) and software interrupts to be distinguished and serviced efficiently (col. 2 lines 17-20).

As to claim 7, Moyer further teaches the interrupt control circuit includes an interrupt factor register (e.g. register 160) having a plurality of bits (0 -> N-1) in which the allocation and setting of bits of an interrupt factor are programmable and a circuit (172) for outputting an interrupt signal (Fig. 2 and col. 5 lines 42-65).

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (6,180,864) (hereinafter Furuhashi '864') in view of Falik et al. (6,532,507) (hereinafter Falik), and further in view of Furuhashi et al. (6,427,181) (hereinafter Furuhashi '181').

As to claim 8, the argument above for claim 5 applies. Furuhashi '864' further discloses the memory device connected to the first bus is a RAM (e.g. DRAM 5, or RAM 21-1 in DSP 8-1). However, Furuhashi '864' and Falik do not disclose a program at start-up for operating the contained CPU loaded by the external host from an external memory connected to the second bus when the CPU contained LSI is started. Furuhashi

'181' teaches the external CPU (2) loads the DRAM (11) with a bootstrap program for operating the contained CPU (12 or 31-1) from external memory (3) connected to the second bus (22) (CPU 12 executes an initializing process according to the bootstrap program, Fig. 2 and col. 2 line 60 to col. 3 line 40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include loading a bootstrap program transferred from the external CPU for operating the contained CPU when the CPU contained LSI is started as taught by Furuhashi '181' in the system of Furuhashi '864' and Falik to increase the signal processing capability of the computer apparatus and allow a program in such an apparatus to be easily modified which is an improvement over prior art where a bootstrap program for graphic computers and video entertainment systems is fixedly stored in a built-in ROM (col. 1 lines 44-55).

8. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (6,180,864) (hereinafter Furuhashi '864') in view of Falik et al. (6,532,507) (hereinafter Falik), and Furuhashi et al. (6,427,181) (hereinafter Furuhashi '181'), and further in view of Ishii et al. (5,890,210). (hereinafter Ishii).

As to claims 9-10, the argument above for claim 8 applies. Furuhashi '864' further teaches the bus adjusting circuit includes a writing data register (FIFO 31) and writes data to be written in the RAM in the writing data register (FIFO 31 temporarily stores the data that is output from host CPU 57 and outputs it to DRAM 5 via bus 12, col. 3 lines 26-32). However Furuhashi '864' does not explicitly disclose a writing address register wherein the external CPU sets the address of the RAM to the writing address

register and the writing address register is incremented every time data is written in the writing data register. Ishii teaches implementing writing address register (42) (Fig. 1) in a buffer area (HDC 41 and buffer RAM 3) for transferring data to/from a memory (Medium 9) wherein the address of the memory 9 to be written is set in the writing address register 42 and the writing address register 42 is incremented every time data is written in the buffer 3 (Fig. 17 and col. 12 line 56 to col. 13 line 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a writing address register in the buffer area (host interface 1) of Furuhashi '864' which can be incremented every time data is written in the buffer area as taught by Ishii to so that the operation of writing data into the memory is effected when write data is transferred to the buffer (col. 13 lines 28-32) and also the write address does not have to be set by the sending master every time data is transferred (col. 13 lines 14-27).

***Response to Arguments***

9. Applicant's arguments filed 04/12/2006 have been fully considered but they are not persuasive:

a. Regarding Applicant's argument of the drawing objection, the Examiner agreed that the specification does support a device having multiple contained CPUs (as argued by Applicant, page 5 of the Remarks), however, the claims recited a detailed connection of the contained CPUs such as "***a first bus*** connected to the ***first contained CPU***; ***a second bus*** connected to ***the second CPU***; ***a first adjusting circuit*** disposed between ***the first bus and the second bus***..." which is not shown in any drawing. None of the figures

show a LSI comprising two CPUs, wherein the first CPU connected to the first bus, the second CPU connected to the second bus... as claimed. It is brought to Applicant's attention that the drawings must show every feature of the invention specified in the claims (37 CFR 1.83(a)).

b. Regarding Applicant's argument "the Host bus 55 is always coupled to the CPU bus 11 via direct bus. Thus, whenever the CPU is coupled to the main bus 12, Host bus 55 is also coupled to the main bus regardless of whether or not the Host CPU 57 is permitted to access a device coupled to the main bus 12. As a result, Furuhashi does not satisfy the recited limitation that in the CPU contained LSI device, the second bus can ONLY be connected to the first bus WHEN the external CPU is permitted to access the device: it is noted that Applicant is arguing one of the possible embodiments in Furuhashi wherein host 57 may directly access DRAM 5 and other devices via direct bus 33 (col. 3 lines 18-20). However, nowhere in Furuhashi teaches Host bus 55 is coupled to the main bus ***regardless of whether or not*** the ***Host CPU 57*** is ***permitted*** to access a device coupled to the main bus 12. Instead, Furuhashi clearly discloses "The ***bus arbiter 2 arbitrates the use rights to main bus 12***. For example, when there is request for data transfer from host CPU57..." (col. 3 lines 21-25). Thus, CPU 57 (or any devices) who wants to couple to bus 12 for service must obtain the access permission from the arbiter. Therefore, the second bus can ONLY be connected to the first bus WHEN the external CPU is PERMITTED to access the device.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Trisha Vu
Examiner
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